AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1-25. (canceled)

26. (new) A multiplexer circuit comprising:

a first passgate circuit coupled to receive a first set of four input bits and a first set of four corresponding select signals, the first set of select signals to select one of the first set of four input bits to be passed through a corresponding passgate and onto a first node;

a first default circuit also coupled to receive the first set of four select signals as inputs to a first OR gate and output of the first OR gate coupled to a gate of a first P-type transistor, which is activated to couple a default supply voltage onto the first node, if the first set of select signals select none of the first set of input bits to be passed through to the first node;

a second passgate circuit coupled to receive a second set of four input bits and a second set of four corresponding select signals, the second set of select signals to select one of the second set of four input bits to be passed through a corresponding passgate and onto a second node;

a second default circuit also coupled to receive the second set of four select signals as inputs to a second OR gate and output of the second OR gate coupled to a gate of a second P-type transistor, which is activated to couple the default supply voltage onto the second node, if the second set of select signals select none of the second set of input bits to be passed through to the second node; and

a NAND gate coupled directly to the first and second nodes without a use of a buffer between the first node and a first input terminal of the NAND gate and between the second node and a second input terminal of the NAND gate, the NAND gate to receive either one of the first set of inputs bits or one of the second set of input bits for output from the NAND gate, in which the default supply voltage is coupled to the NAND gate from other of the first or second node not having an input bit selected for output

from the NAND gate, and in which direct coupling of the first and second nodes to the NAND gate generates the output from the NAND gate with reduced time delay in response to an eight bit width input to the multiplexer circuit.

27. (new) The multiplexer circuit of claim 20 wherein the default supply voltage is Vdd.